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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,709	04/04/2001	Hideki Kabune	1-129	1768

23400 7590 05/14/2004

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RESTON, VA 20190

EXAMINER

YANCHUS III, PAUL B

ART UNIT	PAPER NUMBER
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2116

5

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/824,709

Applicant(s)

KABUNE ET AL.

Examiner

Paul B Yanchus

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 April 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1, 2, 3 and 6 in Paper No. 4 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al., US Patent no. 5,339,446, in view of Nakajima, US Patent no. 5,721,887.

Regarding claims 1 and 6, Yamasaki et al. teaches an electronic control apparatus comprising:

a plurality of power source circuits [POWER OUTPUT in Figure 1] providing a plurality of power sources of a plurality of different voltages [outputs of power supply section, column 3, lines 5-10]; and

a microcomputer [COMPUTER SYSTEM in Figure 1], wherein any one of the plurality of power sources is used as a power source of the microcomputer [POWER OUTPUT in Figure 1 and column 3, lines 60-67].

Yamasaki et al. also teaches detecting if any one of the plurality of power sources is not set to a voltage in respective specified ranges by checking whether the plurality of power sources are respectively set to the voltages in the specified ranges [column 3, lines 17-25].

Yamasaki et al. teaches stopping the power supply when it is detected that any of the power sources output a voltage that is outside of a normal range [column 3, lines 17-25], but does not explicitly teach resetting the microcomputer when a voltage abnormality is detected. Nakajima teaches detecting when a voltage supplied to a microcomputer falls below a normal level and resets the microcomputer if the voltage remains below a normal level for a predetermined period of time [column 2, lines 16-57].

It would have been obvious to one of ordinary skill in the art to incorporate Nakajima's teaching of resetting a microcomputer when the supplied voltage is outside of a normal range into the microcomputer taught by Yamasaki et al. because it would prevent erroneous operation of programs executed by the microcomputer [Nakajima, column 2, lines 45-55].

Regarding claim 2, Yamasaki et al. teaches that the power source circuits have a first power output circuit outputting a first voltage [+12 V] that is applied to a peripheral circuit [RS232C port, column 3, lines 45-67], and a second power output circuit outputting a second voltage [+5 V] that is lower than the first voltage and applied to the reset control unit, the oscillation circuit and the CPU [computer system, column 3, lines 45-67]. Yamasaki et al. does not explicitly show an analog-digital converting unit, a reset control circuit and an oscillation circuit, but it is well known in the art that conventional computer systems have an analog-digital converting unit, a reset control unit to reset the CPU and an oscillation circuit to provide a clocking signal to the CPU.

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Yamasaki et al. and Nakajima, as described above, teach detecting if any one of the plurality of power sources is not set to a voltage in respective specified ranges and resetting the microcomputer if one of the power sources is not set to a voltage in the respective specified ranges.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al., US Patent no. 5,339,446 and Nakajima, US Patent no. 5,721,887, in view of Carter, US Patent no. 6,298,449.

Yamasaki et al. and Nakajima, as described above, teach detecting if any one of the plurality of power sources is not set to a voltage in respective specified ranges and resetting the microcomputer if one of the power sources is not set to a voltage in the respective specified ranges. Yamasaki et al. and Nakajima do not explicitly teach detecting if any of the plurality of power sources is not set to a current in respective specified ranges. Carter teaches detecting if current being input to a computer deviates from a predetermined range [column 5, lines 20-43, column 6, lines 8-23 and column 9, lines 14-16].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Yamasaki et al. and Nakajima with the teachings of Carter. According to Carter, abnormal current levels can be a strong indication of a computer failure [column 5, lines 25-27]. Detecting abnormal current levels in addition to abnormal voltage levels in a computer system provides an extra level of fault detection to which leads to improved system reliability.

Conclusion

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The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sommer, US Patent no. 5,303,143, teaches monitoring a current source.


McCarten et al., US Patent no. 6,559,812, teaches resetting a computer system if the supply voltage drops below an acceptable level.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (703) 305-8022. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
May 12, 2004



REHANA PERVEEN
PRIMARY EXAMINER